Design, Simulation and Application of Buck Converter with Digital PI Controller

Hasan Sucu, Taner Goktas, Muslum Arkan

Abstract—In this paper, a dc-dc buck converter with digital PIcontrolled is analyzed and designed considering all design parameters such as inductance current variation, output voltage ripple etc. The designed dc-dc buck converter provides stable output voltage against to load changes and output voltage variations. Buck converter control method relies on voltage mode controlled PWM (Pulse width Modulation) with digital PI (Proportional Integral) controller. The design criteria, operating mode selection, suitable material selection, etc. of low cost and high-performance buck converter are explained in detail. Finally, the designed converter is carried out experimentally and the experimental results shows the effectiveness of designed converter under different load profiles.

Index Terms—Buck Converter, PWM (Pulse Width Modulation), digital PI controller (Proportional Integral), voltage mode controller.

I. INTRODUCTION

W ITH THE widespread use of renewable energy sources, it is obvious that dc microgrid networks and smart home systems will take place more in our lives in the future. In addition, with the developments in battery technology, the number of electric vehicles and portable devices is constantly increasing. It seems that dc voltage is the trend of the future. Thus, high quality, reliable, adaptable and efficient DC voltage conversion is of great importance.

Buck converters, one of the circuits widely used for dc voltage conversion in power electronics applications, reduce the input dc voltage at the rate of duty cycle. These types of converters are widely used in motor drive applications [1], electric vehicle charging stations [2], li-ion battery supplied application [3], led lamp driver applications [4], dc micro-grid applications [5], wind energy systems [6], photovoltaic systems [7], server applications [8]. Their important advantages are that

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they can be designed at high powers, be highly efficient and have a low price/performance ratio.

Buck converters generate output voltage by switching methods called pulse width modulation (PWM) and pulse frequency modulation (*PFM*). While frequency modulation technique is used in low load conditions under 50mA, pulse width modulation technique is generally used in heavy load conditions over 100mA [9-10]. In the pulse width modulation technique, the semiconductor power switch is switched in the specified duty cycle by keeping the switching frequency constant.

However, changes in input voltages and output load and nonlinear properties of circuit elements make it difficult to obtain a constant output voltage in a constant duty cycle in open loop dc to dc converters. Therefore, a feedback loop is required to achieve output voltage regulation with fast line and load transient response. Buck converters are classified into voltage mode and current mode according to the feedback control loop [11]. Compensation circuits are used because simple control loops will drive the circuit to oscillation. Compensation circuits can be implemented as analog or digital to improve the stability and transition time [12]. The digital controller has some abilities such as faster switching, easy to implementing algorithm etc. [13-14]. Digital control is applied through the Microprocessors, *FPGA* (Field Programmed Gates Array) and Custom *IC* Design.

Linear control methods such as *PI* control [15] and nonlinear control methods such as sliding mode [16] and fuzzy logic [17] are used to ensure stability in output voltage. Each of these control methods for various applications has some advantages and disadvantages in itself. Classical linear feedback is most commonly used for duty cycle control, especially the well-known *PID* control [18]. The dynamic and steady state response are effective in PID control method. [19]. On the other hand, linear controllers like *PI/PID* are easy to design and implement in real physical systems and a well-tuned *PI* controler in the buck converter will provide good performance [20].

In this study, the analysis, selection of design parameters, control, simulation and experimental application of a about 10 *Watt* microcontroller based buck dc-dc converter are conducted. Dynamic performance features such as high efficiency and low output current ripple have been taken into account in the converter design. The designed converter is analyzed in *MATLAB@Simulink* environment and the compatibility of the simulation results with the design parameters are checked. Using the *Altium Designer* program,

the converter PCB-card design is realized. The Texas Instrument *TMS320F28379D series DSC* control card is used for digital *PI* control. The accuracy of the design criteria and simulation results are proved with the experimental results.

II. ANALYSIS OF BUCK CONVERTER AND DETERMINATION OF DESIGN PARAMETERS

The basic circuit diagram for the dc-dc buck converter with an output voltage lower than the input voltage is shown in Fig.1. In the first stage of the design, it is necessary to determine the operating modes and circuit parameters. As it is known, in switching mode converters operate continuously, discontinuously and in threshold conditions depending on whether the inductance current falls to zero or not. Since the inductance current does not decrease to zero in a converter operating in a continuous current mode, the output-inductance current ripple may be at a lower value compared to other operating modes. In the discontinuous current mode, it has advantages in terms of absorbing the energy in inductance, especially at high powers.

In a buck converter operating in continuous current operating mode, as it is seen in Fig.2, when the S-switch is in on state, the diode will switch off because the diode is reverse polarized and during this time (DT) input circuit will provide energy to both the load and the inductance and the inductance current will increase with a certain slope (See. Fig.1a). When the S-switch is in off state, the voltage on the inductance will change direction (1-D) and the inductance current will provide current to the output during T and complete its circuit through the diode. (See Fig.1b). Since the average capacitor current in steady state is zero (open circuit with direct voltage), the average inductance current is equal to the average output current. Where Drepresents duty cycle and T represents the switching period. The voltage falling on the inductance is equal to the difference between the input voltage (V_i) and the output voltage (V_o) when the switch is in on state. The voltage falling on the inductance is equal to the $-V_{a}$ voltage when the switch is in off state.

In the converter operating in continuous current mode, there is an equivalence as in Eq. (1) between the output and the input voltage, by taking advantage of the fact that the energy accumulated in the inductance and the energy consumed in the inductance in the ideal situation are equal to each other and the average inductance voltage is zero.

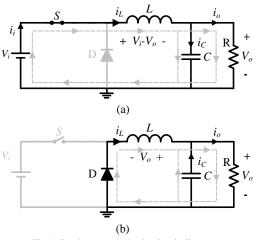


Fig.1. Buck converter basic circuit diagram

 i_L i_L

(a) S-switch on state, (b) S-switch off state

TABLE I. BUCK CONVERTER DESİGN PARAMETERS

Parameters	Value
Input voltage, V _i	48
Output voltage, Vo	12
Switching frequency, kHz	100
Output power, W	9.6
Output voltage fluctuation, $\Delta V_o/V_o$	0.05

TABLE II. BUCK CONVERTER COMPONENTS VALUE

Parameters	Value
Load resistor, Ω	15
Inductance, μH	100
Output Capacitor, μF	26

$$V_o = DV_i$$

$$D = \frac{t_{on}}{T}$$
(1)

Here, the t_{on} indicates the time the switch remains in transmission. As seen in Eq. (1), there is a ratio between the output voltage and the input voltage as much as the duty cycle (0 < D < 1). Since the duty cycle is less than 1, the output voltage will always be lower than the input.

The design criteria of the buck converter operating in continuous current mode with a power of approximately *10 Watt* are given in Table I. By selecting the high switching frequency, the dimensions of the components to be used in the circuit are kept low.

Considering the parameters in Table I, the duty cycle D = 0.25 and the output resistance is $R = 15\Omega$. The minimum

inductance (L_{min}) value required for the converter to operate in continuous current mode can be calculated by Eq. (2) [21]:

$$L_{\min} = \frac{(1-D)R}{2f} = 56.25 \mu H \tag{2}$$

A converter operating at L_{min} value calculated in Eq. (2) operates under threshold condition. A value slightly larger than this specified value should be selected to operate in continuous current mode. In the design, this value was increased by 25% and the inductance value in Eq. (3) was determined.

$$L = 1.25 \times L_{\min} = 70.31 \mu H \tag{3}$$

The inductance current ripples depends on the inductance voltage and the inductance value. If the inductance current ripple is calculated considering the time the switch remains in conduction:

$$\Delta i_L = \left(\frac{V_i - V_o}{L}\right) DT = 1.28 A \tag{4}$$

Depending on this ripple amount (Δ_{iL}), the maximum inductance current and minimum inductance curret can be easily calculated as in Eq. (5) and in Eq. (6) by considering the inductance current waveform in Fig. 2.

$$I_{L\max} = \overline{I_L} + \frac{\Delta I_L}{2} = 1.44A \tag{5}$$

$$I_{L\max} = \overline{I_L} - \frac{\Delta I_L}{2} = 0.16A \tag{6}$$

Buck converter output voltage ripple should generally be less than 1%. Since the inductance current ripples are also seen in the capacitor current, the capacitor value that ensures the output voltage ripple ($\Delta V_0 / V_0$) to be at the desired value can be calculated as in Eq. (6) [20]:

$$C_0 = \frac{1 - D}{8L(\Delta V_0 / V_0) f^2} = 26 \,\mu F \tag{7}$$

The values calculated for the components to be used in the circuit are combined in Table II.

Considering the circuit design criteria and design parameters, the values of the elements used in the circuit in a basic buck converter operating in continuous current mode were determined. In the next section, closed loop control of the Buck converter is explained.

III. VOLTAGE MODE CONTROLS OF BUCK CONVERTER

The block diagram of the voltage mode digital *PI* controlled buck converter consisting of power and feedback stages is shown in Fig.3. Voltage mode control is based on sensing the output voltage. Output voltage V_0 is sensed and converted by a signal conditioning circuit to a suitable voltage value for the analog input channel and applied into the *DSP* via the analog input channel. The sensed output voltage digitized by ADC is compared with the reference voltage V_{ref} . The obtained error e[n] is tried to be minimized by *PI* control. The output K₂e[n]of this controller is used to generate duty cycle in *DPWM*

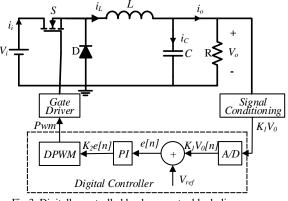


Fig.3. Digitally controlled buck converter block diagram

module. *DPWM* is used as a D/A converter to provide the duty cycle and generates *PWM* signal. The *PWM* is used to turn the switch on and off through the driver.

The close loop controller is designed to ensure that the output voltage V_0 follows the reference voltage V_{ref} . *PI* control is widely used for feedback control in buck converters due to its easy implementation and low cost. *PI* control can be defined by the following transfer function.

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau$$
(8)

Here u(t) represents the control signal and e(t) the error. K_p represents the proportional gain and K_i the integral gain. The proportional term aims to reduce the error by multiplying the error coming from the system with a coefficient. For a small error in large values of K_p there may be large variations in output. This may cause system instability. Compensation for input distortions is slow at small values of K_p . This causes delayed regulation of the controller. This is undesirable in most applications [12]. Integral means finding the area of the error. In each duty cycle, the error is summed by multiplying the coefficient K_i . The integral term reduces the small error left from the proportional controller. The performance of a closed loop converter is highly affected by the controller parameters. Methods such as empirical methods, analytical methods, methods based on optimization are developed in the literature to set the K_i and K_p parameters.

Microcontroller is used to generate the PWM signal in digitally controlled switched power supplies. The amplitude of the PWM signal generated by the microcontroller is low. For this reason, a driver circuit should be used between the PWM output of the microcontroller and the gate of the power switch to charge and discharge the gate capacitance of the high side switch. This driver circuit will increase the voltage in the 0-5V range at the microcontroller output to the required voltage level for switching [22]. The gate driver is important for fast switching of the power element, reducing power losses associated with switching, and reducing parasitic capacitances at switch nodes. In addition, the use of a gate driver will protect the microcontroller from voltage spikes and noise, and at the same time, the gate load will reduce power losses and thermal stress in the microcontroller by moving the power losses from the microcontroller to the drive [23-24].

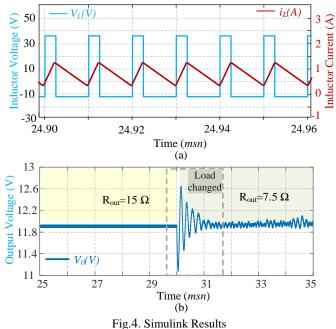
Driving techniques such as floating supply gate drive, transformer coupled drive, charge pump drive, bootstrap drive can be used in buck converters to switch the semiconductor power switch [25-26]. However, the most appropriate solution for driving semiconductor power switches in buck converters is to use the bootstrap drive circuit in terms of cost and simplicity [23].

IV. SIMULATION MODEL AND RESULTS

In order to verify the efficiency of the designed digitally controlled buck converter, the *Matlab @ Simulink* model in Fig.5. is created before its experimental implementation. The simulation model has circuit parameters based on Table I and Table II. The simulation model has been operated under full load conditions, continuous current mode, closed loop control. In the simulation model, suitable oscilloscopes are used to observe the inductance current, inductance voltage, output current, input and output voltages.

In the simulink model, the output voltage is detected and compared to the 12V reference voltage. The obtained error is tried to be minimized by PI control. PI control parameters K_i and K_p can be determined using PID tuning tool in Matlab @ Simulink. K_p value is 0.02752 and K_i value is 8.1185. The saturation block limits the error signal at the output of the PI control to the upper and lower saturation values. The saturation block output is compared with the sawtooth waveform generated from the repeating sequence block to determine the duty cycle. The frequency of the sawtooth waveform corresponds to the desired converter switching frequency 100kHz. Mosfet switches when the error value is greater than the triangular wave. With the step block, the switch is activated 0.03 seconds after the operating moment, the load of the circuit is increased to 20W and the output voltage response of the circuit against load changes is observed.

Fig.4. shows the results of the simulation model created. As



(a) Inductance voltage and Inductance current (b) Output voltage

 TABLE III.

 RISE TIME AND OVERSHOOT VALUE FOR DIFFERENT K_P AND K_i

 VALUES

Parameters	Rise time (Sn)	Overshoot (V)
$K_p = 0.02752, \ K_i = 8.1185$	0.022	5.1
$K_p = 0.05504, K_i = 8.1185$	0.015	6.8
$K_p = 0.01376, K_i = 8.1185$	0.030	3.4
$K_p = 0.02752, K_i = 16.237$	0.011	5.3
$K_p = 0.02752, K_i = 4.05925$	0.041	5.0

seen in Fig.4a, while the switch is in on state, the inductance current increases at a certain slope, it decreases when the switch is off state. In addition, inductance current ripple is approximately the same as design values calculated in Eq. (5) and in Eq. (6) and the current value is always greater than zero. This situation indicates that the designed converter works in continuous current mode. Fig.4b. shows the output voltage. It is seen at the output by decreasing the input voltage at the rate of duty cycle. When the load is increased to 20W, it is seen that the *PI* controller ensures the output voltage stability. The ripple in the output voltage is reduced to the value specified in Table II with the appropriate capacitor value.

The simulation results of the rise time and overshoot value of the output voltage for different values of K_p and K_i are given in Table III. $K_p = 0.02752$ and $K_i = 8.1185$ are used as reference values. First, the K_i value are kept constant and overshoot and rise time are observed for half and twice the K_p value. Afterwards, the K_p value are kept constant and overshoot and rise time are observed for half and twice the K_i value. It is seen from the simulation results that when K_p value is increased by keeping K_i value constant, rise time decreases and overshoot increases, and when K_p value is decreased, rise time increases and overshoot decreases. In addition, when the K_i value is increased by keeping the K_p value constant, it is seen that the rise time decreases and the overshoot increases, and when the K_i value is decreased, the rise time increases and the overshoot decreases.

V. EXPERIMENTAL SETUP AND RESULTS

In order to experimentally examine the dynamic performance of the designed converter, an experimental circuit setup consisting of the input power source, the designed buck converter and the microcontroller was established. Fig.6. shows the designed buck converter and circuit setup. *TI-C2000* series *F28379D DSC* control card, one of the high-performance microcontrollers of Texas Instruments was used to perform the voltage mode digital *PI* control of the buck converter. By using the output voltage applied to the analog inputs of this card, the duty cycle is adjusted in software and hardware. In addition, the *PWM* signal, inductance current and output voltage were observed using a digital oscilloscope.

The circuit block diagram of the digital voltage mode controlled buck converter is shown in Fig.7. It consists of five section. The 48V-12V section provides the + 12V voltage required for the mosfet driver supply and the 12V-3.3V section provides the + 3.3V voltage required for the opamp driver circuit supply.

The signal conditioning circuit consisting of voltage divider resistor circuit and voltage follower opamp circuit is used to

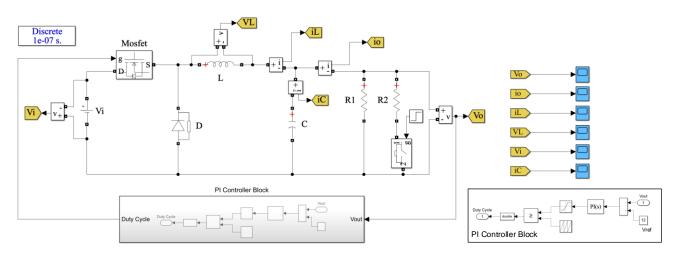
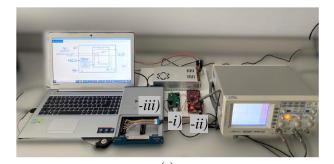
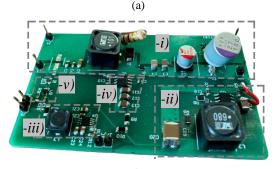


Fig.5. Digitally Controlled Buck Converter, Matlab @ Simulink Model

convert the output voltage to suitable voltage values for the ADCIN channels of the TMS320F28379D DSP and to protect the ADCIN channels of the TMS320F28379D DSP. The output voltage is detected and applied to the analog input channel of the DSP.The analog input voltage applied to the ADCIN channels of the TMS320F28379D DSP needs to be kept in the range of 0V-3.3V. For this purpose, in voltage mode control, the output voltage V_0 is scaled by a voltage divider resistors circuit.

Since the feedback voltage is compared to an internal reference voltage to adjust the output voltage, any inaccuracy in the feedback voltage creates inaccuracies in the output voltage. Low noise and wide gain bandwidth opamp driver circuit with internal electrostatic discharge(ESD) protection circuit are used to protect ADC inputs. Opamp driver circuit





(b) Fig. 6. a) Test Bench Setup -i) Buck Converter -ii) F28379D DSC -iii) NI Data Acquisition Board b) Buck converter PCB Layout -i) Buck Circuit -ii) 48V-12V Circuit -iii) 12V-3.3V circuit -iv) Gate Driver Circuit -v) Signal Condition Circuit

provides low / stable output impedance.

The opamp is connected as a unity gain, non-inverting buffer. This opamp circuit is a voltage follower circuit with high input impedance and low output impedance. Since there is no voltage difference between the opamp inputs, the output voltage V_0 is the same as the input voltage V_{in} . In addition, the V = 3.3V voltage required to feed the opamp circuit is provided from the PCB board by designing a suitable voltage regulator circuit.

A bootstrap gate driver circuit is designed to drive the mosfet. Gate Driver IC are chosen to provide the required peak current. With gate driver circuit, about 5V PWM signal is converted to + VCC value and power switch is turned on and off properly. Also, the VDD = 12 V voltage required to feed the gate driver IC. With the suitable voltage regulator circuit, the input voltage is converted to the required 12V voltage for the gate driver IC supply. The gate driver IC is physically placed close to the power switch to minimize the effects of high frequency switching noise.

The Altium Designer program is used for the PCB drawing of the designed buck converter. In the PCB converter board drawing, the stray capacitance effect around the mosfet is reduced by selecting appropriate current paths and thickness. Short and wide current paths are used to reduce leakage inductance in loops with high current variation (di/dt). In nodes where the voltage change rate (dv/dt) with respect to time is high, it is tried to minimize the conductor area in the node in order to reduce the leakage capacitance.

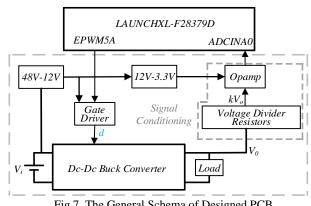
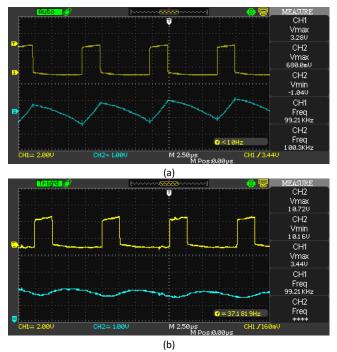
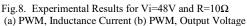
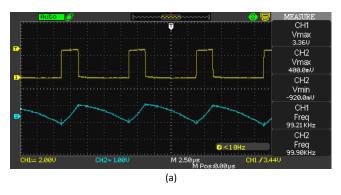


Fig.7. The General Schema of Designed PCB







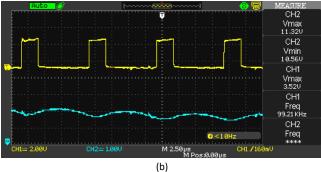


Fig.10. Experimental Results for Vi=48V and R=20 Ω (a) PWM, Inductance Current (b) PWM, Output Voltage

A ground plane is used to reduce the effect of return current noise of a devices on other components and to minimize voltage drops caused by inductance and resistance with the short connections in the return path. By keeping the trace length, resistance are reduced and the susceptible to *EMI* is decreased.

Aluminum housed power resistors with different resistance values of 50W are used as load resistors: 10Ω , 15Ω , 20Ω , 25Ω . Thus, the stability of the circuit against output load changes is

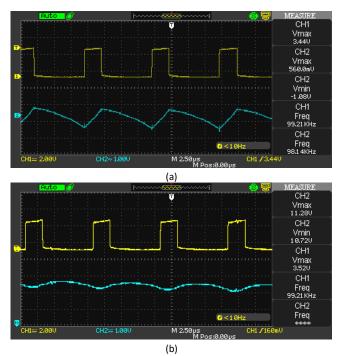
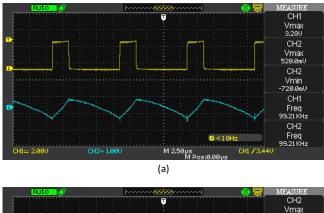


Fig.9. Experimental Results for Vi=48V and R=15 Ω (a) PWM, Inductance Current (b) PWM, Output Voltage



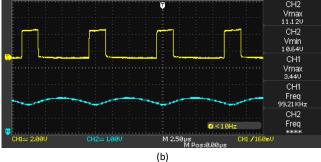


Fig.11. Experimental Results for Vi=48V and R= 25Ω (a) PWM, Inductance Current (b) PWM, Output Voltage

observed. The Code Composer Studio (CCS) software development environment is used to digitize the analog voltage applied to the *ADCIN* channels of the *TMS320F28379D DSP* and to perform *PI* control. The codes developed with this program are compiled and loaded into the processor. $K_p = 0.5$ and $K_i = 0.001$ are chosen to obtain the desired control response with *PI* control. While determining K_p and K_i values, the effects of changing control parameters such as rise time, settling time,

overshoot, steady state error and stability are taken into consideration.

Fig.8, Fig.9, Fig.10. and Fig.11. shows the experimental results for different load resistance with Vi =48V. The amplitude of the switching signal produced by TI-F28379D is about 3.3V. Switching frequency is 100kHz. This generated switching signal is connected to the power mosfet gate driver circuit as an input. As seen in Fig.8(a), Fig.9(a), Fig.10(a) and Fig.11(a), inductance current ripple match calculated values and Simulink results. Inductance currents are 1.044A, 0.733A, 0.547A and 0.435A for 10Ω , 15Ω , 20Ω , 25Ω resistors, respectively. When the inductance current waveforms are examined carefully, it is seen that the converter operates in continuous current mode. The output voltage contains only a small ripple caused by the parasitic parameters in the converter. As seen in Fig.8(b), Fig.9(b), Fig.10(b) and Fig.11(b), measurements show an under/overshoot voltage of -0.38V. The output voltage ripple is within permissible limit. In addition, the converter is stable, working at a switching frequency of 100 kHz without significant noise.

It is seen from the experimental results that the average values of output voltages are almost the same for all load resistance. The designed controller sets the duty cycle depending on load resistance.

Fig.12. shows the thermal performance of designed converter with 15 Ω load resistor. This snapshot is taken at 25^oC ambient temperature. The section of the *PCB* with the maximum heat is shown in red. This section includes a low power 1 Ω resistor used to measure inductance current. This resistor is not included in the designed circuit and is added just before measurement. The yellow portion indicates the heat on inductance.

In order to calculate the efficiency of the circuit, the experimental results measured with a multimeter are given in Table IV. The input power is calculated as 8.92 *W* and the output power is 7.657*W*. The power efficiency is calculated as follow:

$$\%\eta = \frac{P_0}{P_i} \times 100 = 85.8 \tag{9}$$

As seen, the efficiency of the system is lower than 100% due to on-state resistances of mosfet and diode.

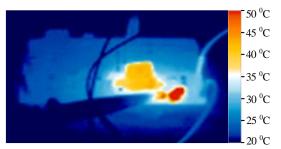


Fig.12. Thermal performance of designed converter

TABLE IV. BUCK CONVERTER EXPERIMENTAL RESULTS

Parameters	Value
Input voltage, V	48.22
Input current, A	0.185
Output voltage, V	11
Output current, A	0.696

VI. CONCLUSION

In this study, the analysis, simulation and experimental application of a microcontroller-based dc-dc buck converter is carried out. The architecture and circuit implementation details are discussed in detail. The design parameters are verified with simulations and experiments. It is observed that the designed converter provides important design criteria such as high operating frequency, low output current ripple, and continuous current mode. Closed loop control technique is applied to the designed converter to hold the output voltages constants against to the load changes. The presented simulation and experimental results show the effectiveness of the developed controller in terms of overshoot limitations and accuracy.

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